Customer No.: 31561
Application No: 10/605,198
Docket NO.:11422-US-PA

Claim Amendment

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A split gate flash memory cell, comprising:

a substrate, wherein a device isolation structure is configured in the substrate to define an active region;

a selective gate structure, disposed on the substrate, wherein the selective gate structure comprises, sequentially from the substrate, a first gate dielectric layer, a selective gate and a cap layer;

a spacer, disposed on a sidewall of the selective gate structure;

an interlayer dielectric layer, disposed on the substrate, wherein the interlayer dielectric layer comprises an opening, disposed on one side of the selective gate structure, exposing a portion of the selective gate structure, the substrate and the device isolation structure;

a floating gate, disposed in the opening, wherein a portion of the floating gate extends to cover a surface of the interlayer dielectric layer;

a tunneling dielectric layer, disposed between the substrate and the floating gate;

a control gate, formed over the floating gate and disposed in the opening, filling the opening and extending above the selective gate structure;

a second gate dielectric layer, disposed between the floating gate and the control gate;

a source region, disposed in the substrate at a side of the control gate that is not adjacent to the selective gate; and

a drain region, disposed in the substrate on a side of the selective gate that is not adjacent to the control gate.

2. (original) The memory cell of claim 1 further comprises an erase gate, disposed on the interlayer dielectric layer above the source region, wherein a portion of the erase gate covers the floating gate.

3. (currently amended) The memory cell of claim ~~1~~2, wherein the second gate dielectric layer is further disposed between the erase gate and the floating gate.

4. (original) The memory cell of claim 1, wherein the control gate extends to cover the floating gate above the selective gate structure.

5. (original) The memory cell of claim 1, wherein an etching selectivity of the cap layer and the spacer is different from that of the interlayer dielectric layer.

6. (currently amended) A split gate flash memory device, comprising:

a substrate, wherein a device isolation structure is configured in the substrate to define an active region;

a first selective gate structure and a second selective gate structure, disposed respectively on the substrate, wherein each of the first selective gate structure and the second selective structure comprises a first gate dielectric layer, a selective gate and a cap layer;

a spacer, disposed on a sidewall of the first selective gate structure and the second selective gate structure;

an interlayer dielectric layer, disposed on the substrate, wherein the interlayer dielectric layer comprises a first opening and a second opening, and the first opening and the second opening are configured between the first selective gate structure and the second selective gate structure, and the first opening exposes a portion of the first selective gate structure, the substrate and the device isolation structure, and the second opening exposes a portion of the second selective gate structure, the substrate and the device isolation structure;

a first floating gate and a second floating gate, disposed in the first opening and the second opening, respectively, and extended to cover a surface of the interlayer dielectric layer;

a tunneling dielectric layer, disposed between the first floating gate and the substrate, and between the second floating gate and the substrate;

a first control gate and a second control gate, wherein the first and the second control gates are disposed in the first opening and the second opening, respectively, the first and the second control gates fill the first opening and the second opening, respectively, and the first and the second control gates extend above the first selective gate structure and the second selective gate structure, respectively;

an erase gate, disposed on the interlayer dielectric layer that is in between the first control gate and the second control gate, wherein a portion of the erase gate covers the first floating gate and the second floating gate;

a second gate dielectric layer, disposed between the first floating gate and the first control gate and between the first floating gate and the erase gate, and between the second floating gate and the second control gate and between the second floating gate and the erase gate;

a source region, disposed in the substrate between the first control gate and the second control gate;

a first drain region and a second drain region, configured in the substrate, at one side of the first selective gate that is not adjacent to the first control gate, and at one side of the second selective gate that is not adjacent to the second control gate; and

a bit line, disposed on a substrate and electrically connected to the first drain region and the second drain region.

7. (currently amended) The memory ~~cell~~ device of claim 6, wherein the second gate dielectric layer comprises a silicon oxide/silicon nitride/silicon oxide layer.

8. (currently amended) The ~~method~~ memory device of claim 6, wherein the first control gate covers the first floating gate above the first selective gate structure, and the second control gate covers the second floating gate above the second selective gate structure.

9. (currently amended) The ~~method~~ memory device of claim 6, wherein the bit line is electrically connected to the first drain region and the second drain region through a contact plug, respectively.

10. (currently amended) The ~~method~~ memory device of claim 6, wherein an etching selectivity of the cap layer and the spacer is different from that of the interlayer dielectric layer.